REMARKS

In response to the Office Action dated 21 January 2003, the applicant requests reconsideration of the above-identified application in view of the following remarks. Claims 2, 3, 24-28, 41-48, 50-52, and 65-68 are pending in the application, and are rejected. None of the claims have been amended.

Telephone Interview

The applicant thanks Examiner Eckert for the telephone interview granted on Thursday, 17 April 2003, between himself and the applicant's representative Mr. Mates (Reg. No. 35,271). The substance of this response was discussed during the interview.

Double Patenting Rejection

Claims 2, 3, 24-28, 41-48, 50-52 and 65-68 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims of co-pending Application No. 08/902, 843. The applicant will address this rejection when the claims are otherwise indicated as allowable.

Rejections of Claims Under §103

Claims 2, 3, 24-28, 41-48, 50-52 and 65-68 were rejected under 35 USC §103(a) as being unpatentable over Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata) in view of Sugita et al. (JP Patent No. 08-255878, Sugita) and Burns et al., *Principles of Electronic Circuits* , pp. 382-383 (Burns). The applicant respectfully traverses.

The MPEP states the following with regard to rejections under 35 USC § 103: "To establish a *prima facie* case of obviousness ... there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." MPEP 2143. A Federal Circuit opinion states that the suggestion or motivation to combine references must be found in the prior art. MPEP 2143 citing *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991). In addition, the Federal Circuit, in *In re Lee*, 61 USPQ2d 1430 (Fed. Cir. 2002), requires that the

suggestion or motivation to combine references "be based on objective evidence of record." The Federal Circuit also indicated that the suggestion or motivation must be specific. 61 USPQ2d at 1433. *In re Lee* is referenced in MPEP 2143.01, page 2100-125.

The applicant respectfully submits that the combination of Sakata, Sugita, and Burns is not supported by sufficient objective evidence as is required by *In re Lee*.

The Office Action states that the motivation for combining Sakata, Sugita, and Burns is that "the source, drain, and channel regions allow individual floating gate devices to be formed in an array....[t]he use of the source/drain/channel regions for such programming is well known in the art." Office Action, page 5. The office action did not cite evidence in the record, such as one of the references, that supports the above-stated motivation for combining Sakata, Sugita, and Burns. The Office Action did not cite evidence showing that the HJ structure of Sakata must have a source and a drain in a substrate to be formed in an array.

The Office Action states that "it is considered obvious to form the control gate of Sakata et al. from polysilicon." Office Action, page 6. The motivation making this substitution is stated above: "[t]here are several advantages of using polysilicon as a control gate, for example, polysilicon can be doped to a low resistivity and is able to withstand higher temperatures so that it is unaffected during subsequent annealing steps." Office Action, page 6. The Office Action has not identified objective evidence in the record to support this motivation to modify Sakata as is required by *In re Lee*.

The evidence already in the record does not support the modification of Sakata proposed in the Office Action.

The diode structure of Sakata is fundamentally different from the structure of a traditional transistor such as those shown in Sugita and Burns. The words source, drain, and channel do not appear in Sakata. Those skilled in the art understand that a conventional transistor has a channel region that induces the transport of only one type of majority charge carrier, a p-type channel for holes or an n-type channel for electrons. In contrast, the diode structure of Sakata receives both electrons and holes. "By applying a negative (positive) gate bias, holes (electrons) are injected from the substrate into the a-Si:H layer through the graded a-SiC:H layer and recombine with the stored electrons (holes) and thus the memory is erased." Sakata, text bridging columns 1 and 2.

Burns emphasizes the different principles of operation of a floating gate transistor such as disclosed by Sugita and the principles of operation of the HJ diode structure of Sakata quoted above. Burns describes the programming of a floating gate transistor with the language: "[e]lectrons are accelerated, ...and acquire enough energy to enter the conduction band of the gate oxide layer. There they are attracted by the positive potential on the select gate, and many of them lodge on the floating gate." Burns, page 383. Burns then describes the erasure of the floating gate transistor with UV light: "[t]he UV light imparts photon energy to the electrons, allowing them to escape through the oxide layer." Burns, page 383. Unlike the operation of the HJ diode structure of Sakata, only electrons are involved in programming and erasing a floating gate transistor.

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." MPEP 2143.01. The modification of Sakata proposed in the Office Action might change the principle of operation of Sakata.

The applicant has submitted pages from two textbooks, Sze and Streetman, that support the applicant's position. Sze defines a heterojunction as "a junction formed between two dissimilar semiconductors." Sze, page 122. Heterojunctions are used in bipolar transistors and optoelectronic devices such as lasers, light-emitter diodes, photodetectors, and solar cells. Sze, page 122. Sakata refers to this class of semiconductor devices when he states that "[a]lthough the application of the heterojunction (HJ) composed of hydrogenated .... has been limited to optoelectronic devices." Sakata, page 688, column 1. Sze and Streetman show several examples of heterojunction structures, and none of them show a source region in a substrate, a drain region in the substrate, and a channel region between the source region and the drain region in the substrate that the Office Action finds obvious to add to the HJ structure of Sakata.

With reference to the "Response to Arguments" section starting on page 10 of the Office Action, there are statements in Sakata referring to memory devices. For example, Sakata states that "the present structure can be used as a component of dynamic random access memories (DRAMs) [4] at room temperature." Sakata, page 689, column 1.

The applicant has submitted a paper entitled *Multi-Day Dynamic Storage of Holes at the AlAs/GaAs Interface* by Qian et al. (Qian). Qian shows a p+GaAs/AlAs/n-GaAs capacitor

structure in Figure 1 and uses a capacitance-voltage (CV) technique to measure the storage time of holes. Qian, Abstract and Figure 2. In the conclusion Qian notes the CV behavior of the capacitor structure and claims that it is appropriate for use in a dynamic RAM memory device.

The applicant notes that Sakata emphasizes the CV characteristics of Sakata's sample diode. Sakata, page 688, column 2. The applicant respectfully submits that Sakata seems to suggest in the text quoted above that the heterojunction structure may be used in a capacitor in a DRAM device.

The Office Action states on page 11 of the above argument "[t]he implication of these arguments and secondary references seems to be that the device of Sakata cannot be formed with a source and drain ....though Sakata do state that their invention may be used in a DRAM, that does not undermine or negate its use in a floating gate structure, which structure does have sources and drains." The applicant respectfully submits that the burden is on the Patent Office to establish a *prima facie* case of obviousness, and the arguments made by the applicant to show that a *prima facie* case has not been supported.

Sakata also appears to suggest that the heterojunction structure can be used in a floating gate device as in this statement: "the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices." Sakata, page 688, column 1. Sakata also says that "heterojunctions on c-Si can be applied to electrically programmable and erasable memory devices." Sakata, abstract.

Sakata also refers to a paper: "Capasso *et al.* [2] [Capasso] reported similar memory devices based on AlGaAs/GaAs HJ." Sakata, page 688, column 2. Sakata is referring to the earlier statement in the same paragraph, quoted above, that "the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices." Sakata, page 688, column 1.

Capasso, of record, reports AlGaAs/GaAs floating-gate memory devices. Capasso, abstract. However, Capasso does not show a picture of the device.

The applicant has submitted a paper entitled *Anisotropic Thermionic Emission of Electrons Contained in GaAs/AlAs Floating Gate Device Structures* by Lott et al. (Lott-1 according to the Office Action). Lott shows in Figure 1 the mask set and epitaxial layers of a floating gate transistor. Lott-1 refers to the transistor as "[o]ur test vehicle (Fig. 1) has a vertical structure similar to that of Capasso *et al.* " Lott-1 is referring here to the same Capasso paper that Sakata refers to in the quote above from page 688, column 2. The transistor structure shown

in Figure 1 of Lott-1 is probably similar to what Sakata is referring to when Sakata says that "the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices." Sakata, page 688, column 1. The HJ structure of Sakata may be contemplated by Sakata as being in a floating gate transistor having the same orientation of elements shown in Figure 1 of Lott-1. This is more likely than the combination of Sakata and Sugita put forward in the final Office Action.

The transistor of Lott-1 has a source, a drain, a gate, and a floating gate. However, the source, drain, and gate shown in Lott-1 are formed next to each other on a superlattice, and the floating gate of Lott-1 is on the other side of the superlattice. A barrier separates the floating gate of Lott-1 from the channel of Lott-1. The floating gate of Lott-1 is between the source and drain on one side and the channel on the other side, and separates the source and the drain from the channel.

The transistor structure of Lott-1 is substantially different from that of Sugita, even though both have elements with the names source, drain, and floating gate. Sakata and Figure 1 of Lott-1 are linked by their reference to the same paper by Capasso. Lott-1 specifically says that the structure of Figure 1 is similar to that of Capasso. Sakata specifically says that Capasso reported a similar memory device. If there is a suggestion in Sakata for the use of its HJ structure in a floating gate device, it is most probably the floating gate transistor shown by Lott-1. The transistors of Lott-1 and Sugita are substantially different, and therefore the applicant respectfully submits that the statement in Sakata is **not** a suggestion or motivation to combine Sakata, Sugita, and Burns.

The structures of the transistors of Sugita and Lott-1 are substantially different, and this is evidence that their principles of operation are different. Sakata refers to the use of Sakata's HJ structure in a floating gate device similar to that shown by Lott-1, a transistor that probably has a different principle of operation than the transistor of Sugita. Lott-1 is evidence that an addition of elements from Sugita to the HJ diode structure of Sakata would change the principle of operation of Sakata, and therefore teaches away from a combination of Sakata and Sugita.

On the other hand, Sakata may be merely expressing the hope that the diode structure can be used in some unspecified type of memory device. The C-V plot of Sakata shows a "large hysteresis" that may be used as a memory window. Sakata, column 2. While the hysteresis shown in the C-V plot may be used to create a device to store data, this is **not** a suggestion that

the HJ diode structure of Sakata can and should be combined with elements of the floating gate transistors of Sugita or Burns.

The Office Action states on page 14 that motivation was found to use a source and drain in the Si substrate of Sakata. The applicant demonstrated above that the Office Action did not cite evidence to support this motivation as is required by *In re Lee*. The Office Action also stated on page 14 that the reference in Sakata to "similar memory devices" is not limited to the structure of Capasso, but encompasses all devices that exploit "band engineering principles to store charge" regardless of structure. However, the rejection combining Sakata, Sugita, and Burns proposes a specific structural change to Sakata, and the MPEP and the case law cited above require a specific suggestion in the prior art to make this modification. A showing of a specific suggestion in the prior art for the proposed structure is necessary to establish a *prima facie* case of obviousness.

The Office Action has not identified sufficient objective evidence in the record to support the combination of Sakata, Sugita, and Burns as is required by *In re Lee*.

The applicant respectfully submits that a *prima facie* case of obviousness of claims 2, 3, 24-28, 41-48, 50-52 and 65-68 has **not** been established in the Office Action, and that claims 2, 3, 24-28, 41-48, 50-52 and 65-68 are in condition for allowance.

Claims 2, 3, 24-28, 41, 45, 46, 50, 65 and 68 were rejected under 35 USC §103(a) as being unpatentable over Lott et al. (*Charge Storage in InAlAs/InGaAs/InP Floating Gate Heterostructures*, Electronics Letters 26, pp. 972-973, July 5, 1990, referred to in the Office Action as Lott-2) in view of Sakata. The applicant respectfully traverses.

Claim 24 recites a transistor comprising a source region in a substrate, a drain region in the substrate, a channel region between the source region and the drain region in the substrate, and a gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

Sakata shows in Figure 1 a heterojunction (HJ) diode structure comprising c-Si, a layer of hydrogenated amorphous silicon carbide (a-SiC:H), a layer of hydrogenated amorphous silicon (a-Si:H), another layer of a-SiC:H, and Al. Sakata, page 689, column 1. Sakata is deficient as a reference in that Sakata does not show a source region in a substrate, a drain region in the

substrate, and a channel region between the source region and the drain region in the substrate as are recited in claim 24.

Lott-2 shows an InAIAs/InGaAs/InP floating gate heterostructure including a source, a drain, a floating gate, and a sense channel.

Lott-2 is also deficient as a reference in that, while Lott-2 shows the sense channel, it is a separate layer in the heterostructure of Lott-2, and is not shown as being part of the same structure as the source and the drain of Lott-2. Therefore, even as combined, Sakata and Lott-2 do not show a channel region between a source region and a drain region in a substrate as is recited in claim 24.

The Office Action states the motivation for combining Lott-2 and Sakata is the statement in Sakata that "Capasso *et al.* [2] reported similar memory devices based on AlGaAs/GaAs HJ. However, excessive leakage current made it impossible to electrically erase the memories and a visible light pulse was instead used to erase the memory." Sakata, page 688, column 2.

This statement is not a specific suggestion to combine Lott-2 and Sakata. First of all, it refers to the specific device of Capasso, and not to III-V heterojunctions in general or the device in Lott-2. Second, it does not appear to be a suggestion to substitute parts of Sakata into the heterojunction of Capasso, but to replace it entirely. There is no indication in this statement that putting a layer or two of a silicon material into Capasso's heterojunction would solve the leakage problem.

Beyond the statement, it is not clear what parts of the HJ structure of Sakata that the Office Action proposes to add to Lott-2, or what layers in Lott-2 are to be replaced. The Office Action is not specific about what technical modification is proposed, and therefore the motivation provided is also not specific.

The MPEP also states the following with regard to rejections under 35 USC § 103: "To establish a *prima facie* case of obviousness ... there must be a reasonable expectation of success." MPEP 2143. A Federal Circuit opinion states that the reasonable expectation of success must be found in the prior art. MPEP 2143 citing *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991). The Office Action is proposing to combine a silicon-based device (Sakata) with a InAIAs/InGaAs/InP heterostructure (Lott-2). The Office Action itself recognizes that the silicon-based device of Sakata and III-V devices of Capasso and Lott-1 have different structures.

Office Action, page 12. The Office Action has not provided objective evidence from the prior art that such a combination would have a reasonable expectation of success as is required by *In re Lee* and *In re Vaeck.*

The applicant respectfully submits that a *prima facie* case of obviousness of claim 24 has **not** been established in the Office Action, and that claim 24 is in condition for allowance. Claims 25-28 are dependent on claim 24, and recite further limitations with respect to claim 24. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that a *prima facie* case of obviousness of claims 25-28 has **not** been established in the Office Action, and that claims 25-28 are in condition for allowance.

Claims 2, 3, 41, 45, 46, 50, 65 and 68 recite elements similar to those recited in claim 24. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that a *prima facie* case of obviousness of claims 2, 3, 41, 45, 46, 50, 65 and 68 has **not** been established in the Office Action, and that claims 2, 3, 41, 45, 46, 50, 65 and 68 are in condition for allowance.

Claims 42, 43, 47, 48, 51, 52, 66 and 67 were rejected under 35 USC §103(a) as being unpatentable over Lott-2 in view of Sakata and Burns. The applicant respectfully traverses.

The Office Action states that it would have been obvious to form the device of Lott-2 and Sakata with the polysilicon control gate of Burns. "The motivation for doing so is that there are several advantages of using polysilicon as a control gate, for example, polysilicon can be doped to a low resistivity and is able to withstand higher temperatures so that it is unaffected during subsequent annealing steps." Office Action, page 10. The Office Action has not identified objective evidence in the record to support this motivation to combine Sakata, Lott-2, and Burns as is required by *In re Lee.*

The applicant respectfully submits that a *prima facie* case of obviousness of claims 42, 43, 47, 48, 51, 52, 66 and 67 has **not** been established in the Office Action, and that claims 42, 43, 47, 48, 51, 52, 66 and 67 are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 21 day of April, 2003.

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Signature